

Keysight U4301B
PCI Express® 3.0
Analyzer Module

Data Sheet



Introduction

Keysight solutions for PCIe Gen1 to Gen3 analysis and emulation

- PCIe Gen1 (2.5GT/s), Gen2 (5GT/s), and Gen3 (8GT/s) support
- x1, x2, x4, x8, x16 link width
- LTSSM analysis and power state testing
- Flow Control credit and performance analysis
- PCIe, NVMe, AHCI, and Configuration space decoding and analysis
- Compact AXIe modular system configuration

Overview

Product description

Keysight Technologies' high speed U4301B PCI Express® 3.0 analyzer module is a protocol analyzer supporting all PCI Express® applications from Gen1 through Gen3 and speeds, including 2.5 GT/s (Gen1) and 5.0 GT/s (Gen2) through PCIe 8 GT/s (Gen3) and with link widths from x1 to x16. The U4301B analyzer captures and decodes PCI Express data and displays it in a packet viewer window.

The U4301B analyzer is a blade that is installed in an AXIe two slot M9502A or five slot M9505A.

Probing is provided by the U4321A solid slot interposer probe, U4324A flying lead solder down probe, or the U4322A mid bus probe based on Keysight's equalization snoop probe (ESP) technology.

Gain insight into the equalization process and all of the state transitions with views that can be customized to meet your requirements. The analyzer LTSSM overview can pinpoint specific training sequence issues through easy to interpret analysis results.

Keysight's Transactional decoder includes a transactional viewer that allows the designer to select transactional queues and performance information from the analyzer's NVMe transaction overview pane. This organizes the transactions by direction or by queue to follow the data flow across the interface, with one-click control. Individual PRP (Physical Region Page) lists contain all of the key information of the NVMe queues, allowing designers to quickly review and validate the data flows over the PCIe connections.

The performance analysis package includes the real data throughput calculations, with response-time measurement of the PCIe data flow. It allows designers to measure and understand throughput performance, PCIe response times, and other operational measurements that provide the insight needed to optimize device performance.

Complementary PCIe stimulus and response testing of the PCIe system is accomplished with the addition of the U4305A PCIe Gen3 exerciser.

Overview (continued)



Analysis and debug



- Support for Gen1 through Gen3, x1 through x16 link width
- 8 GB of capture buffer per module
- Non-intrusive probing that leverages ESP technology

Industry leading probes



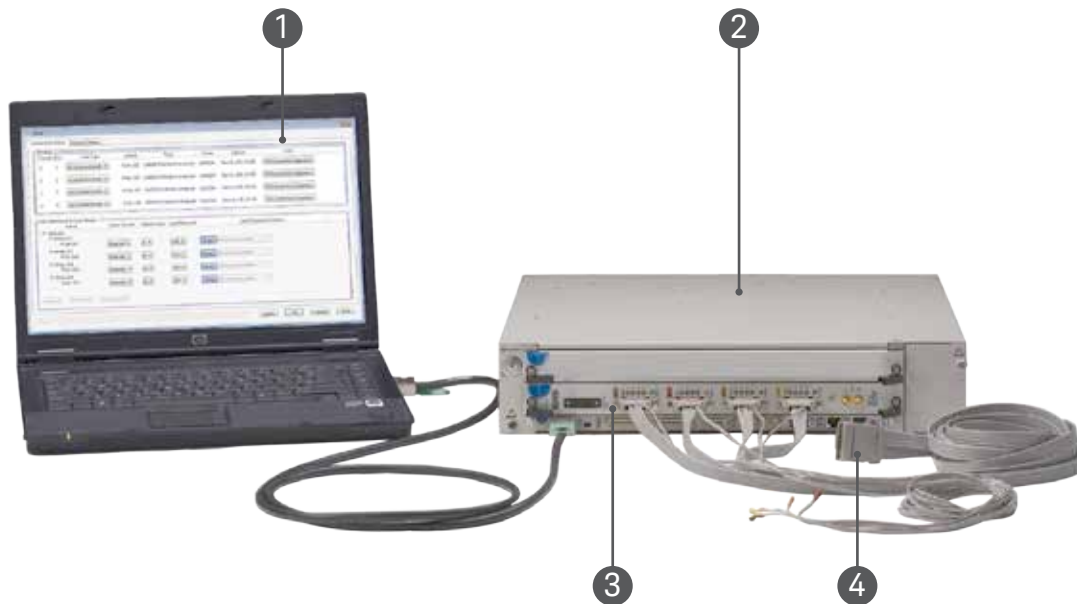
- The mid-bus probe supports x1 to x16 unidirectional or x1 to x8 bidirectional
- The solid slot interposer will support x1 to x16 unidirectional or bidirectional
- The flying lead solder down probe offers support for x1 and x2 bidirectional capability on a single probe. Other standard lane width configuration support is x4, x8, & x16
- The M.2 interposer supports testing of M/B-M PCIe solid state drives (SSDs)
- SFF-8639 interposers can be used with solid state drives (SSDs) with either single or dual link support

Stimulus and test U4305A exerciser



- Support for Gen1 through Gen3 and link widths of x1 through x16
- Link testing from x1 through x16, using automated LTSSM exerciser
- PCIe, MR-IOV, and SR-IOV stimulus response testing
- NVMe Root Complex emulation for test and verification of NVMe devices
- Protocol test card (PTC) to measure PCIe Gen3 DUT port and system BIOS specification compliance as defined by the PCI SIG standards

System Architecture Overview



1. PC controller to manage and interact with the system
2. 2-slot modular chassis
3. U4301B protocol analyzer module controlled via M9536A embedded controller or by PCIe link to external PC
4. U4322A soft touch mid-bus probe 3.0

Configuration

Step 1	<ul style="list-style-type: none"> – Order the U4301B analyzer module. Standard configuration is x1 linkwidth, 5 Gbps, 8 GB capture buffer – Upgrade linkwidth to x4, x8 or x16 – Upgrade to 8GT/s
Step 2	<ul style="list-style-type: none"> – Order a modular chassis – Recommended chassis is the Keysight M9502A 2-slot AXIe chassis or optionally the Keysight M9505A 5-slot AXIe chassis
Step 3	<ul style="list-style-type: none"> – Select a PC controller—Keysight recommends the M9536A embedded controller—or select an external PC that meets the performance requirements as specified in the PXI and AXIe Modular Instrumentation, Tested Computer List Technical Note (http://literature.cdn.keysight.com/litweb/pdf/5990-7632EN.pdf).
Step 4	<p>Order the probe for your measurement application</p> <ul style="list-style-type: none"> – U4321A solid slot interposer 3.0: Order the option for the number of lanes to be tested – U4322A mid bus probe based on Keysight soft touch technology – U4324A flying lead solder down probe: Order the option for the number of lanes to be tested – U4328A M.2 interposer Socket 3 (M-key) – U4330A SFF-8639 interposer for single or dual link
Step 5	<p>Add the exerciser for stimulus/response testing</p> <ul style="list-style-type: none"> – U4305 exerciser: Order the option for the number of lanes to be tested and software licenses for applications such as end node or root complex emulation, LTSSM, SR/MR-IOV, or NVMe emulation

Note: The slot interposer and exerciser lane width is fixed and is not upgradable due to the connector size being a function of lane width. A smaller lane width probe can be used in a wider lane application, but only those lower lanes will be tested. Keysight does not recommend or support the use of lane converters.

Product Features and Benefits Overview

Decoding and Analyzing PCIe Traffic

Displaying the captured data from the 8GB capture buffers is provided by several different “views” that enable you to see exactly the data that is required. The Packets window decodes each captured packet and enables you to quickly and easily find, filter, and decode the PCIe information of interest. This easy to use view allows you to define the parameters of interest and display the details of each packet.

Sample	Time	Down	Up	Address, Register Number	Completion Status	Length	Payload
548021	62.812768928	MemRd_32		Address=D1C1 01B4		001	
547674	62.812769320		CplD		Successful Completion (SC)	001	0000 0000
548022	62.812769603	MemRd_32		Address=D1C1 01B8		001	
547675	62.812769988		CplD		Successful Completion (SC)	001	0000 0000
548023	62.812933452	MemRd_32		Address=D1C1 01B4		001	
547676	62.812933848		CplD		Successful Completion (SC)	001	0000 0000
548024	62.812934084	MemRd_32		Address=D1C1 01B8		001	
547677	62.812934483		CplD		Successful Completion (SC)	001	0000 0000
548025	62.812934732	MemWr_32		Address=D1C1 01B4		001	2000 0000
548026	62.812935153	MemWr_32		Address=D1C1 01B8		001	2000 0000
547678	62.812935562		MemRd_64	Address=0000 0001 3E64 8DA0		004	
548027	62.812935818		CplD		Successful Completion (SC)	004	0500 0100 0000 0000 00ED 643E
547679	62.812936230		MemRd_64	Address=0000 0001 3E64 ED00		005	
548028	62.812936507		CplD		Successful Completion (SC)	005	2780 6001 0000 0040 0000 0001
547680	62.812936751		MemWr_64	Address=0000 0001 3E64 8440		005	3400 4000 0000 0040 0000 0001
547681	62.812978352		MemWr_64	Address=0000 0001 3E64 8400		007	4120 0000 0500 0000 0000 0001
547682	62.812978464		MemRd_64	Address=0000 0001 3E64 ED80		004	
548029	62.812978780		CplD		Successful Completion (SC)	004	0080 3E3E 0100 0000 0000 0001

Figure 1. This spreadsheet view gives you quick and easy access to your favorite views of PCIe packets.

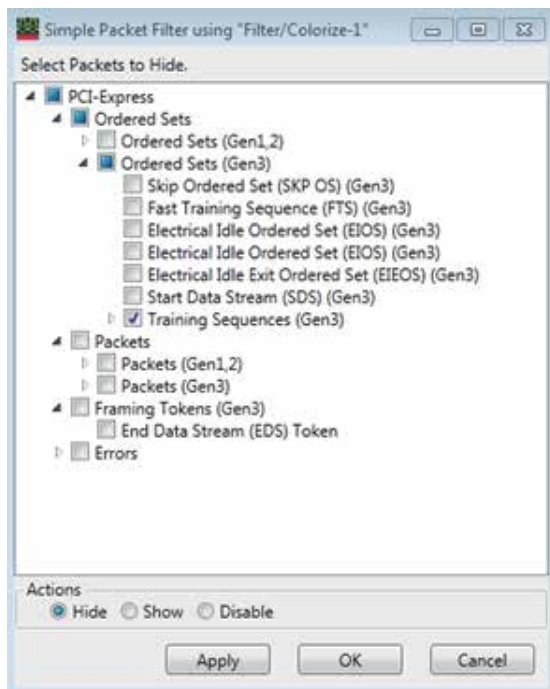


Figure 2. Simple Packet Filter can be used to filter data that has been captured to hide things like training sequences.

Product Features and Benefits Overview (continued)

Decoding and Analyzing PCIe Traffic (continued)

Additional displays give fast understanding of the data in the buffer. Any errors are highlighted in Red and tool tips provide details of the error detected.

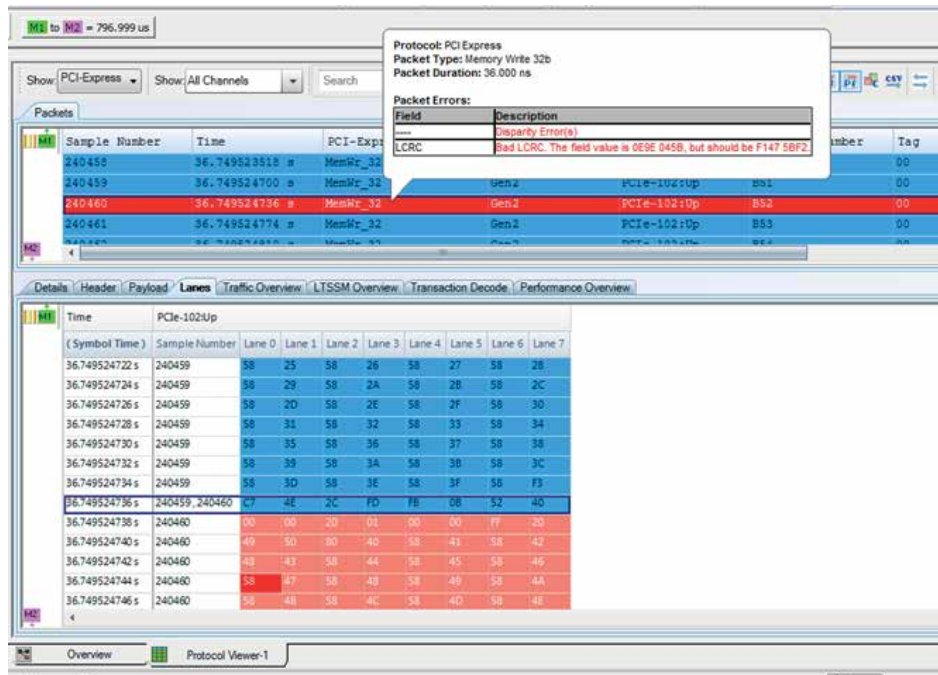


Figure 3. Here a Memory Read packet has a bad LCRC and is directly tied to the Lane view shows which byte and which lane has been corrupted.

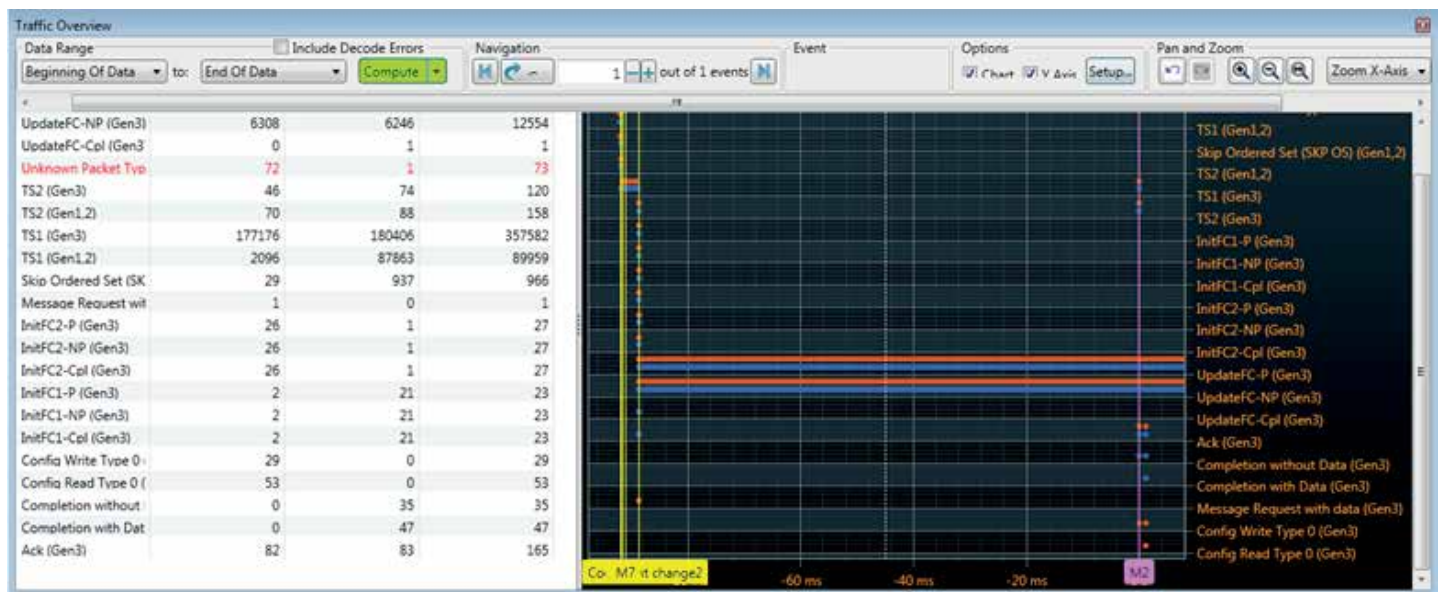


Figure 4. The Traffic Overview shows all of the packets in the capture buffer in a time scale display. Instantly access to any packet by clicking on the graph.

Product Features and Benefits Overview (continued)

Powerful PCIe triggers

The U4301B provides a powerful yet easy to use trigger system uses simple selection of the packet(s) with a drag and drop interface. Then a double click on the packet takes you into a bit level packet definition of the trigger.

Advanced triggers provide a state based trigger event that can be tied to packets, timers, external triggers, or Link state. This enables the capture of those hard to define events that are not defined by a single event packet.

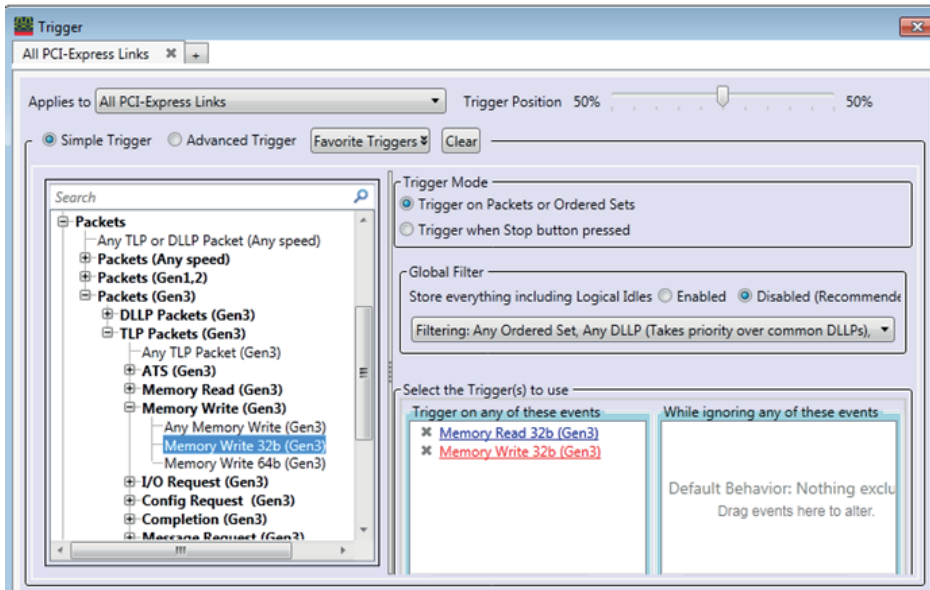


Figure 5. Trigger on Memory Read or Memory Write packet and center the capture buffer around either of these packets.

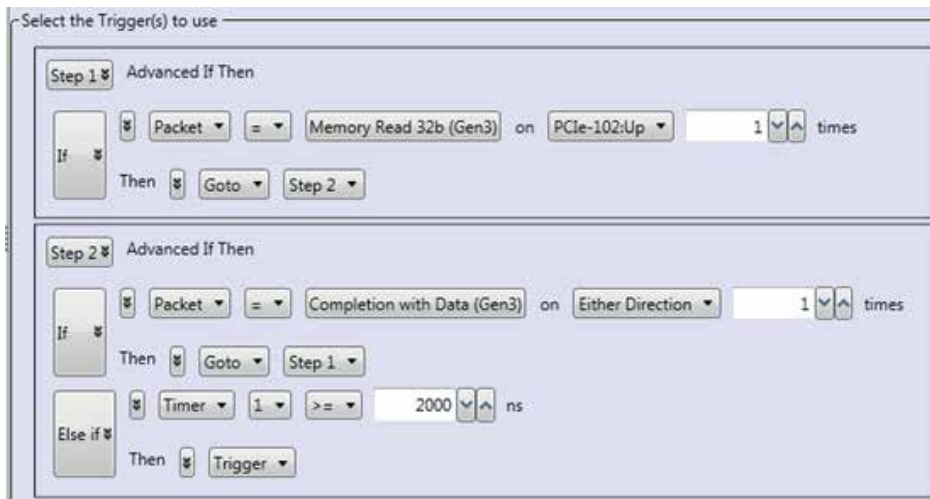


Figure 6. Advanced state based trigger captures the timeout of a completion packet that takes longer than 2 µsecs.

Product Features and Benefits Overview (continued)

NVMe data

Transaction decode

The Transaction Decode tab in the Protocol Viewer window allows you to compute and view transactions decoded from the captured PCIe traffic. The decoding and display of transactions is done as per the relevant storage protocol specifications such as NVMe to help you easily correlate the decoded data to the protocol specifications and evaluate DUT's compliance to these specifications. Transaction decoding of NVMe data includes analysis of the trace to identify all of the relevant transactions types to present a transaction overview table that enables quick and easy navigation of key packet types.



Figure 7. NVMe transaction information provides easy to understand displays of NVMe payloads and PRP messages. Transaction overview of all transactions enables instant access to all messages in the capture trace.

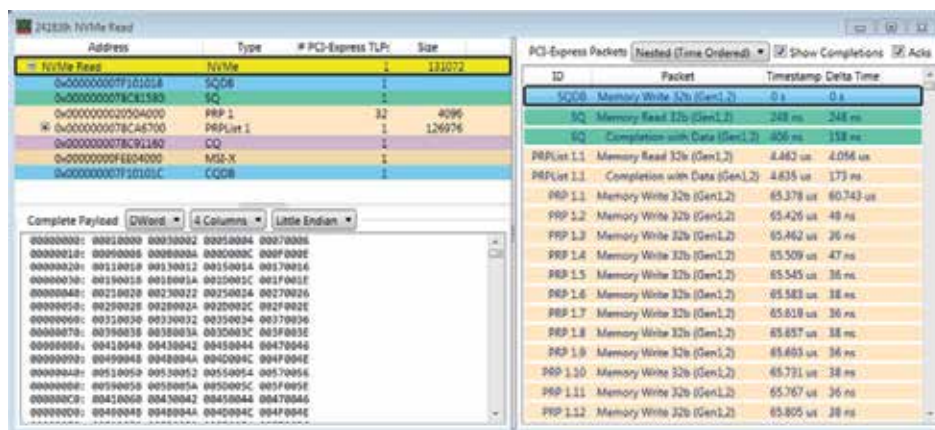


Figure 8. Visualize a decoded NVMe transaction as a super transaction with all its related transactions forming a complete set.

Product Features and Benefits Overview (continued)

AHCI data

AHCI (Advanced Host Controller Interface) and the associated SATA (Serial ATA) commands for storage devices are displayed with the Transaction decode window. By capturing the setup information the configuration is automatic, and the parts of a command are joined together to display the complete operation.

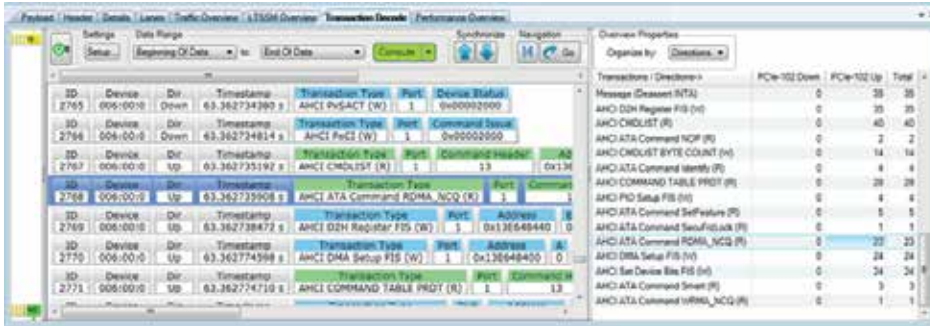


Figure 9. The decoded transactions are a mix of PCIe Config, generic host control, port-specific and SATA commands transactions.

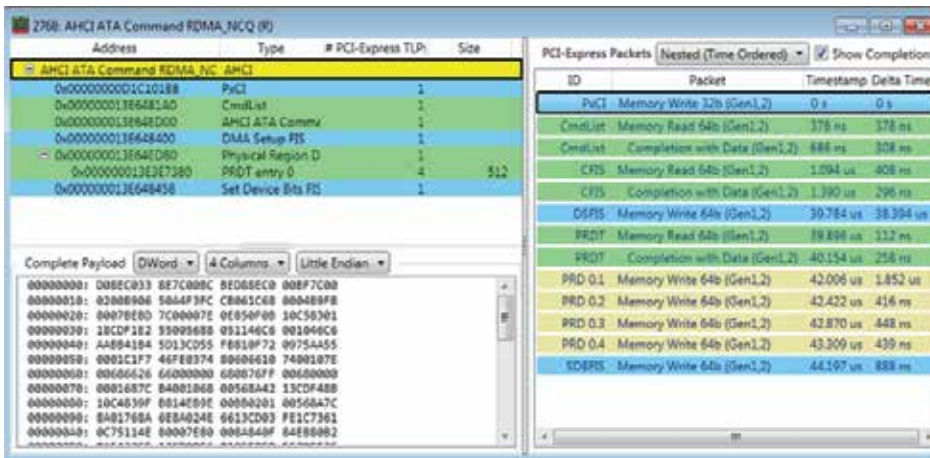


Figure 10. View AHCI transaction displayed in the Transaction Decode tab as a super transaction to visualize its complete set of related transactions.

Product Features and Benefits Overview (continued)

Performance Analysis

Visualize the performance of your PCIe traffic with the built-in statistics provided by the Performance Overview of the U4301B. Over 50 parameters are automatically calculated and with simple checkbox selection all of the performance information is displayed in a time correlated graphical overlay view. The statistical performance of the link latency, utilization, Flow Control credits, is shown with events such as Interrupts and errors.



Figure 13. The statistical performance of the link latency, utilization, Flow Control credits, is shown with events such as Interrupts and errors.

Flow Control Analysis

Flow Control computes and displays the available flow control credits from the data trace that has a bidirectional traffic. Flow control credit level is determined by the Writes and Completions in one direction and the UpdateFC packets in the other direction.



Figure 14. Easily identify credit exhaustion with flow control analysis for data and header flow control analysis.

Product Features and Benefits Overview (continued)

Powerful hardware features ensure capture of important transition events

- Large capture buffer, for long recording sessions with 8 GB per module (x1-x8 bidirectional) and 16 GB for x16 bidirectional
- LEDs to show lane status and speed for fast understanding of current link status



U4301B analyzer module characteristics and specifications

- Environmental specifications as per the main frame except maximum operating temperature = 40 °C
- Trigger input: Input Z = 50 ohms, $V_{max} = 3.3\text{ V}$
- Trigger output: 2.0 V
- Minimum trigger duration: 20 ns

Host PC requirements

Select a PC controller--Keysight is proud to recommend the M9536A embedded controller--or select an external PC that meets the following performance requirements. Keysight has pre-tested a number of external PCs as listed in the PXI and AXIe Modular Instrumentation, Tested Computer List Technical Note (<http://literature.cdn.keysight.com/litweb/pdf/5990-7632EN.pdf>).

- Processor speed: 1 GHz 64-bit (x64) 2 GB minimum available memory running Windows 7 or Windows 8 (64-bit);
- Available hard disc space: 1.5 GB
- Support for DirectX 9 graphics with 128 MB graphics memory recommended, (Super VGA graphics is supported)
- Microsoft Internet Explorer 7 or greater
- Compatible with a PCIe Gen1 x4 interface module

Product Features and Benefits Overview (continued)

Probing

Accurate data recovery with consistent representation of the signal

U4321A slot interposer

- ESP (equalizing snoop probe) technology ensures accurate data recovery in all Gen3 platforms and all link width x1 through x16
- High fidelity signal capture ensures design problems can be reproduced
- Mechanical stabilization for the device under test's (DUT's) end point and to ensure firm PCIe slot connections



Characteristics

- Power: 12 VDC, 1.25A max
- Power supply; Keysight part number 0950-5160
- Input: 100 to 250 VAC, 50 to 60 Hz

Accurate data recovery with flexible use model

U4322A mid bus probe

- Provides signal capture in situations where no PCIe connector is available
- Micro spring-pin probe based on Keysight's soft touch technology provides reliable contact to signal pads
- Independent reference clock per four lanes for maximum layout flexibility



Characteristics

- Input: 25V max or 3 Vrms into 250 ohms
- Temperature: Operating 0 to 40 °C
- Storage -40 to 70 °C
- Humidity: 15 to 95% non-condensing
- Altitude: 3,000 m (10,000 ft)

Accurate data recovery with full channel mapping support and flexible probe points

U4324A flying lead solder down probe

- Provides signal capture in situations where no PCIe slot connector or PCIe standard mid bus footprint is available.
- Low channel count per probe to reduce unnecessary expense for unused channel leads
- Independent reference clock tap for maximum layout flexibility
- Low cost, easily replaceable N5426A zero insertion force (ZIF) tips to maximize probe use life (Includes one set of ten N5426A)



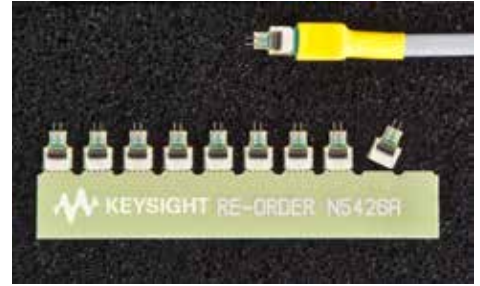
Characteristics

- Input: 10 V max common mode
- Capacitive loading: 0.250 fF
- Temperature: Operating +5 to +40 °C
- Storage: -40 to 70 °C
- Humidity: Operating 80% RH @ 40 °C
- Storage: 90% RH @ 65 °C
- Vibration: 2.09 Grms (5 to 500 Hz random)
- Shock: 1.6 m/s [63 in/s] (2 mS half sine)

Product Features and Benefits Overview (continued)

N5426A ZIF tip kit

- The ZIF tip is a connection accessory used to connect the U4324A flying lead cable to the channel on the DUT
- One side of the ZIF tip connects to the flying lead and is soldered to the DUT on the other end
- The ZIF tip is calibrated to the U4324A flying lead; no impedance changes should take place to the ZIF tip
- 10 ZIF tips per kit



Characteristics

- Input: 10 V max common mode
- Capacitive loading: 0.250 fF
- Temperature: Operating +5 to +40 °C
- Storage: -40 to 70 °C
- Humidity: Operating 80% RH @ 40 °C
- Storage: 90% RH @ 65 °C
- Vibration: 2.09 Grms (5 to 500 Hz random)
- Shock: 1.6 m/s [63 in/s] (2mS half sine)

U4328A PCIe M.2 Socket 2 interposer (M-key)

Enables probing of storage solutions based on the M.2 interconnection standard. The U4328A is perfectly designed to connect between a PCIe Solid State Drive (SSD) and the host that uses the M.2 connection with support for M/B-M PCIe x1, x2 and x4 memory modules (socket 3). The U4328A M.2 Interposer enables monitoring of x1, x2 or x4 PCIe communication links.

The U4328A comes in a kit that supports all standard M.2 sizes. From 2230 through 22110.

U4330A SFF-8639 PCIe interposer (supports single or dual link)

Test Single or Dual port SFF-8639 connections with the U4330A interposer. The SFF-8639 Interposer is a PCIe Storage Interposer that makes it possible to analyze data traffic from PCIe SSD storage devices to PCIe Storage systems using the SFF-8639 connector.

Note: Analyzing SFF-8639 Dual link traffic simultaneously requires 2 - U4301B PCIe analyzer modules.

Product Features and Benefits Overview (continued)

Thorough link testing with the U4305A PCIe exerciser

- Addition of the U4305A provides PCIe,MR-IOV and SR-IOV stimulus response testing
- Predefined LTSSM sequences simplify state transition testing
- Predefined protocol test card (PTC) test cases applied to Lane 0 only, provide specification compliance feedback
- Full speed testing of Gen 1 through Gen 3 systems
- All lane widths supported at full speed
- End point emulation and act as a down stream component (DSC)
- Root complex emulation and act as an upstream component (USC)
- NVMe end point or system testing with compliance test package
- Full API programming and scripting tools



Specifications

- Refer to the U4305A data sheet pub number 5990-8458EN for detailed characteristics and specifications.

Related Keysight Literature

Publication title	Pub number
Hardware and Probing for PCI Express Gen3 User's Guide available at www.keysight.com/find/U4301B	U4301-97000
U4301B PCIe 3.0 Analyzer User Guide	U4301-97001
PCI Express Design and Test – From Electrical to Protocol - Brochure	5989-5594EN
U4305A Protocol Exerciser for PCI Express® 3.0 - Data Sheet	5990-8458EN

Ordering Information

U4301B PCIe Gen3 Analyzer base configuration, 5 GT/s, x1 linkwidth, 8 Gb capture buffer Includes: LTSSM, AHCI, NVMe, and performance analysis

A specific configuration is required to determine the lane width to be tested.

Model number	Description
U4301B-A04	U4301B-A04 Upgrade link width to x4
U4301B-A08	U4301B-A08 Upgrade link width to x8
U4301B-A16	U4301B-A16 Upgrade link width to x16 Note: Analyzing bi-directional x16 requires the purchase of two U4301B modules with U4301B-A16
U4301B-AN3	Upgrade speed to PCIe Gen3, 8GT/s

Modular chassis and computer interface

The recommended chassis is the 2 slot AXIe configuration.

Chassis type	Model number	PC configuration	Interface	Cable
AXIe (recommended)	M9502A 2 slot AXIe	Laptop	M9045B	Y1200B
		Desktop	M9048A	Y1202A

Probe selection

Probe type	Model number	Description
Solid slot interposer 8 Gbps Note: The U4321A interposer probe lane width is fixed and is not upgradable to accommodate different lane widths due to the fact that the connector size is a function of lane width. Keysight does not recommend or support the use of lane converters.	U4321A-A01	Link width x1
	U4321A-A04	Link width x4
	U4321A-A08	Link width x8
	U4321A-A16	Link width x16
Mid-bus probe	U4322A	Mid-bus probe based on Keysight soft touch technology for applications where no standard PCIe connector is available for testing
	U4322A-R05	Set of 5 retention modules
	U4317A	Gen3 to Gen2 mid bus adaptor
Flying lead probe	U4324A	4 channel/probe, Includes qty 1 N5426A
	N5426A	ZIF tip kit (10 pcs)
M.2 interposer socket 3 (M-key)	U4328A	x4 Gen3 passive interposer
SFF-8639 interposer PCIe Gen3	U4330A	Supports single x4 link or dual x2 links (requires 2 analyzer modules)

Analyzer upgrades

Model number	Description
U4301BU-AFP	Analyzer software license upgrade x1 to x4
U4301BU-BFP	Analyzer software license upgrade x1 to x8
U4301BU-CFP	Analyzer software license upgrade x1 to x16
U4301BU-DFP	Analyzer software license upgrade x4 to x8
U4301BU-EFP	Analyzer software license upgrade x4 to x16
U4301BU-FFP	Analyzer software license upgrade x8 to x16

U4305A PCIe Gen3 Exerciser

Refer to the U4305A data sheet pub number 5990-8458EN for detailed characteristics and specifications and ordering instructions.

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